REMARKS

Claims 1-14 were submitted for examination, and all have been rejected. Reconsideration and reexamination of the above-referenced patent application is respectfully requested.

Rejection Under 35 USC §103(a)

Examiner rejected claims 1-14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,097,611 of Samaras et al. (hereinafter referred to as "Samaras") in view of U.S. Patent No. 4,471,408 of Martinez (hereinafter referred to as "Martinez").

35 U.S.C. § 103 Conditions for patentability; nonobvious subject matter

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The prior art combined by the examiner to reject applicant's pending claims as being unpatentable, are owned by the same person, and were owned by the same person or subject to an obligation of assignment to the same person at the time the claimed invention was made. In particular, the present pending application is assigned to the Intel Corp. The cited references Samaras is currently assigned to the Intel Corp., and was assigned or subject to an obligation of assignment to the Intel Corp. at the time the presently claimed invention was made.

Therefore, in accordance with 35 U.S.C. § 103 c, the cited reference Samaras does not preclude the patentability of the applicant's claims.

Conclusion

Applicants respectfully submit that the now pending claims are in condition for allowance.

Respectfully submitted,

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APPENDIX A

VERSION OF SPECIFICATION AND CLAIMS
WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. An integrated circuit (IC) package comprising:

   a substrate including an IC;

   a ground line; and

   an encoded region to provide information based upon selective deposition of solder balls electrically coupled to the ground line.

2. The package of claim 1, wherein the substrate is the substrate of a ball grid array (BGA) package.

3. The package of claim 2, wherein the IC is a processor.

4. The package of claim 3, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

5. The package of claim 4, wherein the encoded region includes at least three solder ball areas.

6. The package of claim 5, wherein the information indicates a voltage supply level for the IC.

7. The package of claim 1, wherein the information indicates a voltage supply level for the IC.

8. An electronic component comprising:

a ball grid array (BGA) package including an encoded region to provide information based upon selective deposition of solder balls; and

a printed circuit board (PCB) coupled to the package.

9. The component of claim 8, wherein the BGA package contains a processor.

10. The package of claim 9, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

11. The package of claim 8, wherein any deposited solder ball in a solder ball area of the encoded region is electrically coupled to a first node of a resistor on the PCB, and a second node of the resistor is electrically coupled to a power trace on the PCB.

12. The package of claim 11, wherein the first node is approximately ground if a solder ball is deposited in the solder ball area, and the first node is approximately Vcc if a solder ball is absent from the solder ball area.

13. The package of claim 12, wherein the encoded region includes at least three solder ball areas.

14. The package of claim 13, wherein the information indicates a voltage supply level for a processor within the BGA package.